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09/447,301	11/23/1999	SATOSHI YOSHIHARA	P99.1899	3648

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EXAMINER	
HANNETT, JAMES M	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/447,301	YOSHIHARA, SATOSHI	
	Examiner	Art Unit	
	James M. Hannett	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/18/2006 have been fully considered but they are not persuasive. The applicant has amended the independent claims to state that there is a readout gate between the image array and the accumulation gate. The examiner asserts that Elabd et al teaches on Column 5, Lines 14-40 the use of a dump drain (35) depicted in Figure 6A that is formed by gates (53,55,35 and 51) This is viewed by the examiner as a readout gate since the charge from the image array needs to pass through the dump drain to be stored in the storage register.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1: Claims 1, 3-8, 11, 12, 15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,196,939 Elabd et al.

2: As for Claim 1, Elabd et al depicts in Figure 4 and teaches on Column 1, Lines 65-68 and Column 2, Lines 12-17 and Column 4, Lines 28-41 and Column 6, Lines 16-20 a solid state image pickup device (31) having a sensor array (13) comprising a plurality of sensors; and a plurality of transfer registers (17A and 17B) for transferring signal charges from the sensors of the sensor array, at least one horizontal-horizontal transfer register; Figure 6A (45 and 47) is formed between said transfer registers (17A and 17B) for storing temporarily and transferring said signal charges: wherein an accumulation gate (33) is provided between said sensor array and

said transfer registers for reading out signal charges from the sensors at a same time, accumulating the signal charges and allocating the signal charges to the transfer registers. Elabd et al depicts in Figure 4 the plurality of transfer registers (17A and 17B) include two transfer registers (17A and 17B) which receive and concurrently transfer charges from at least two Columns (15) of pixels of the image sensor (31). Elabd et al teachers on Column 1, Lines 66-68 and Column 2, Lines 18 and depicts in Figure 4 that only one row is read out of the image sensor at a time and transferred to the storage register (33). Elabd et al further teaches on Column 2, Lines 60-68 and Column 5, Lines 28-35 that the rows of image data transferred to the storage register (33) can be combined using storage site (59) to permit rows to be combined for less detail and a variety of other options. Therefore, in the embodiment discussed on Column 2, Lines 60-68, multiple rows of data are combined in storage register (33) and the then combined pixel value is transferred to transfer registers (17A and 17B). Therefore, transfer register 17A receives charges stored in even-numbered columns from the two mixed rows of image data. And transfer register 17B receives charges stored in odd-numbered columns from the two mixed rows of image data. Therefore, in the thinned readout mode the transfer registers concurrently read out image data from two rows of pixels (the two rows of data are mixed). Elabd et al teaches on Column 5, Lines 14-40 the use of a dump drain (35) depicted in Figure 6A that is formed by gates (53,55,35 and 51) This is viewed by the examiner as a readout gate since the charge from the image array needs to pass through the dump drain to be stored in the storage register.

3: As for Claim 3, Elabd et al depicts in Figures 6B-F and teaches on Column 6, Lines 16-28 The accumulation gate (storage register) creates a difference in electric potential oriented in a direction of transfer. Elabd et al teaches that by clocking the gates overlaying the storage register

the charge will be transferred to the transfer register. Therefore, the storage register sets a difference in electric potential oriented in the direction or the transfer registers.

4: In regards to Claim 4, Elabd et al teaches on Column 4, Lines 42-48 and Column 6, Lines 3-6 that the signal charges of the sensors are stored in the accumulation gate (storage register 33) to be allocated in units of electrical charge each originated by one of the sensors. Elabd et al teaches that the charges from all of the pixels in the image sensor array are output individually by row to the storage register (33), which is viewed as the accumulation gate.

5: As for Claim 5, Elabd et al teaches on Column 4, Lines 42-48 The signal charges of the sensors are allocated to respective transfer registers for each odd sensor and each even sensor of the sensor array. Elabd et al teaches that transfer register 17A receives the charge stored in the even-numbered columns of the transferred row, and transfer register 17B receives charge stored in the odd-numbered columns of the transferred row.

6: In regards to Claim 6, Elabd et al depicts in Figure 4 and teaches on Column 1, Lines 65-68 and Column 2, Lines 12-17 and Column 4, Lines 28-41 and Column 6, Lines 16-20 a method of driving a solid-state image pickup device having: a sensor array (31) comprising a plurality of sensors (13); a plurality of transfer registers (17A and 17B) for transferring signal charges from the sensors of the sensor array; at least one horizontal-horizontal transfer register (45 and 47) formed between said transfer registers (17A and 17B) for storing temporarily and transferring said signal charges; Figure 6A (45 and 47): an accumulation gate (33) provided between the sensor array and the transfer registers, the method comprising the steps of: reading out signal charges from all of the sensors in a row closest to the accumulation gate at the same time; allocating the signal charges of the sensors from the accumulation gate to the transfer registers;

and driving the transfer registers to output the signal charges. Elabd et al depicts in Figure 4 the plurality of transfer registers (17A and 17B) include two transfer registers (17A and 17B) which receive and concurrently transfer charges from at least two Columns (15) of pixels of the image sensor (31). Elabd et al teachers on Column 1, Lines 66-68 and Column 2, Lines 18 and depicts in Figure 4 that only one row is read out of the image sensor at a time and transferred to the storage register (33). Elabd et al further teaches on Column 2, Lines 60-68 and Column 5, Lines 28-35 that the rows of image data transferred to the storage register (33) can be combined using storage site (59) to permit rows to be combined for less detail and a variety of other options. Therefore, in the embodiment discussed on Column 2, Lines 60-68, multiple rows of data are combined in storage register (33) and the then combined pixel value is transferred to transfer registers (17A and 17B). Therefore, transfer register 17A receives charges stored in even-numbered columns from the two mixed rows of image data. And transfer register 17B receives charges stored in odd-numbered columns from the two mixed rows of image data. Therefore, in the thinned readout mode the transfer registers concurrently read out image data from two rows of pixels (the two rows of data are mixed). Elabd et al teaches on Column 5, Lines 14-40 the use of a dump drain (35) depicted in Figure 6A that is formed by gates (53,55,35 and 51) This is viewed by the examiner as a readout gate since the charge from the image array needs to pass through the dump drain to be stored in the storage register.

7: As for Claim 7, Elabd et al depicts in Figure 6A and teaches on Column 5, Lines 14-58 that the transfer registers (17A and 17B) are driven at the same time. Elabd et al teaches that both transfer registers are driven by Signals (H1-H4) Since these signals are supplied to both transfer registers, they are driven at the same time.

8: In regards to Claim 8, Elabd et al teaches on Column 4, Lines 42-48 the signal charges of the sensors are allocated to respective transfer registers for each odd sensor and each even sensor of the sensor array. Elabd et al teaches that transfer register 17A receives the charge stored in the even-numbered columns of the transferred row, and transfer register 17B receives charge stored in the odd-numbered columns of the transferred row.

9: As for Claim 11, Elabd et al depicts in Figure 6A that the accumulation gate (41A and 41B) and the read-out gate (15A) share a common gate electrode. The Figure depicts that the image data is transferred using the same electrode from the image array to the storage register and then to the transfer registers.

10: In regards to Claim 12, Elabd et al depicts in Figure 6A that the step of reading out and the step of allocating are carried out through a common gate electrode. The Figure depicts that the image data is transferred using the same electrode from the image array to the storage register and then to the transfer registers.

11: As for Claim 15, Elabd et al teaches in Table 1 on Column 8, Lines 10-45 that the read-out gate and the accumulation gate are comprised of a same material.

12: In regards to Claim 17, Elabd et al teaches on Column 4, Lines 28-41 and depicts in Figure 6A the readout gate (53,55,35 ands 51) transmits all received signals from the sensor array to the accumulation gate (storage register) and the accumulation gate (storage register) subsequently transfers all of the signals to the transfer registers (17A and 17B). This process occurs if the rows have been selected.

13: As for Claim 18, Elabd et al teaches on Column 4, Lines 28-41 and depicts in Figure 6A the readout gate (53,55,35 ands 51) transmits all received signals from the sensor array to the

accumulation gate (storage register) and the accumulation gate (storage register) subsequently transfers all of the signals to the transfer registers (17A and 17B). This process occurs if the rows have been selected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14: Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,196,939 Elabd et al in view of USPN 5,298,734 Kokudo.

15: As for Claim 9, Elabd et al teaches the claimed invention as discussed in Claim 1. Elabd et al teaches the use of an image sensor that has two horizontal transfer registers that each output odd and even column data respectively. Therefore, the channel stop region between the transfer registers (17A and 17B) have half the number of columns as the transfer registers to allow only half of the columns to pass from transfer register (17A) to transfer register (17B). However, Elabd et al does note teach that the horizontal-horizontal transfer unit has the same number of columns as the transfer registers.

Kokudo teaches in Figure 2 and teaches on Column 4, Lines 10-27 that it is advantageous when designing an image sensor that has two horizontal transfer registers to allow all of the column data from the first transfer register to be transferred to the second transfer register in order to enable the image sensor to perform a progressive scan readout and output two lines of image data simultaneously. Because the entire row of image data can be transferred from the first

transfer register to the second transfer register, it is inherent that the horizontal-horizontal transfer register between them have the same number of columns as the two registers.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the image sensor of Elabd et al to use a horizontal-horizontal transfer register as taught by Kokudo in the invention of Eladb et al to enable the image sensor to perform a progressive scan readout while reading out two rows of image data simultaneously.

16: In regards to Claim 10, Elabd et al teaches the claimed invention as discussed in Claim 6. Elabd et al teaches the use of an image sensor that has two horizontal transfer registers that each output odd and even column data respectively. Therefore, the channel stop region between the transfer registers (17A and 17B) have half the number of columns as the transfer registers to allow only half of the columns to pass from transfer register (17A) to transfer register (17B). However, Elabd et al does note teach that the horizontal-horizontal transfer unit has the same number of columns as the transfer registers.

Kokudo teaches in Figure 2 and teaches on Column 4, Lines 10-27 that it is advantageous when designing an image sensor that has two horizontal transfer registers to allow all of the column data from the first transfer register to be transferred to the second transfer register in order to enable the image sensor to perform a progressive scan readout and output two lines of image data simultaneously. Because the entire row of image data can be transferred from the first transfer register to the second transfer register, it is inherent that the horizontal-horizontal transfer register between them have the same number of columns as the two registers.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the image sensor of Elabd et al to use a horizontal-horizontal

transfer register as taught by Kokudo in the invention of Eladb et al to enable the image sensor to perform a progressive scan readout while reading out two rows of image data simultaneously.

17: Claims 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,196,939 Elabd et al in view of USPN USPN 6,028,299 Hirmada et al.

18: As for Claim 13, Elabd et al depicts in Figure 4 and teaches on Column 1, Lines 65-68 and Column 2, Lines 12-17 and Column 4, Lines 28-41 and Column 6, Lines 16-20 a solid state image pickup device (31) having a sensor array (13) comprising a plurality of sensors; and a plurality of transfer registers (17A and 17B) for transferring signal charges from the sensors of the sensor array, at least one horizontal-horizontal transfer register; Figure 6A (45 and 47) is formed between said transfer registers (17A and 17B) for storing temporarily and transferring said signal charges: wherein an accumulation gate (33) is provided between said sensor array and said transfer registers for reading out signal charges from the sensors at a same time, accumulating the signal charges and allocating the signal charges to the transfer registers. The accumulation gate is viewed by the examiner as the storage register (33). The horizontal-horizontal transfer region is viewed by the examiner as the transfer region (47) that transfers charge between the two transfer registers (17A and 17B). Elabd et al depicts in Figure 4 the plurality of transfer registers (17A and 17B) include two transfer registers (17A and 17B) which receive and concurrently transfer charges from at least two Columns (15) of pixels of the image sensor (31). Elabd et al teachers on Column 1, Lines 66-68 and Column 2, Lines 18 and depicts in Figure 4 that only one row is read out of the image sensor at a time and transferred to the storage register (33). Elabd et al teaches on Column 5, Lines 14-40 the use of a dump drain (35) depicted in Figure 6A that is formed by gates (53,55,35 and 51) This is viewed by the examiner

as a readout gate since the charge from the image array needs to pass through the dump drain to be stored in the storage register. Elabd et al further teaches on Column 2, Lines 60-68 and Column 5, Lines 28-35 that the rows of image data transferred to the storage register (33) can be combined using storage site (59) to permit rows to be combined for less detail and a variety of other options. Therefore, in the embodiment discussed on Column 2, Lines 60-68, multiple rows of data are combined in storage register (33) and the then combined pixel value is transferred to transfer registers (17A and 17B). Therefore, transfer register 17A receives charges stored in even-numbered columns from the two mixed rows of image data. And transfer register 17B receives charges stored in odd-numbered columns from the two mixed rows of image data. Therefore, in the thinned readout mode the transfer registers concurrently read out image data from two rows of pixels (the two rows of data are mixed). However, Elabd et al does not teach that the image array can be directly connected to accumulation gate without any vertical shift registers between them.

Hirmada et al teaches on Column 1, Lines 32-60 and depicts in Figure 1 the use of a linear image sensor in which the accumulation gate 29A is directly connected to the sensor array (22) via a readout gate (ROG). This is capable because the sensor array in Hirmada et al is a linear array and requires no vertical shift register. Linear image sensors are advantageous to use in document scanning systems.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to directly connect the linear sensor of Hirmada et al to the accumulation gate of Elabd et al in order to allow the imaging system of Elabd et al to be used in an image scanning system in which a linear sensor is required.

19: In regards to Claim 14, Elabd et al depicts in Figure 4 and teaches on Column 1, Lines 65-68 and Column 2, Lines 12-17 and Column 4, Lines 28-41 and Column 6, Lines 16-20 a solid state image pickup device (31) having a sensor array (13) comprising a plurality of sensors; and a plurality of transfer registers (17A and 17B) for transferring signal charges from the sensors of the sensor array, at least one horizontal-horizontal transfer register; Figure 6A (45 and 47) is formed between said transfer registers (17A and 17B) for storing temporarily and transferring said signal charges: wherein an accumulation gate (33) is provided between said sensor array and said transfer registers for reading out signal charges from the sensors at a same time, accumulating the signal charges and allocating the signal charges to the transfer registers. The accumulation gate is viewed by the examiner as the storage register (33). The horizontal-horizontal transfer region is viewed by the examiner as the transfer region (47) that transfers charge between the two transfer registers (17A and 17B). Elabd et al teaches the method comprising the steps of: reading out signal charges from all of the sensors in a row closest to the accumulation gate at the same time; allocating the signal charges of the sensors from the accumulation gate to the transfer registers; and driving the transfer registers to output the signal charges. Elabd et al depicts in Figure 4 the plurality of transfer registers (17A and 17B) include two transfer registers (17A and 17B) which receive and concurrently transfer charges from at least two Columns (15) of pixels of the image sensor (31). Elabd et al teachers on Column 1, Lines 66-68 and Column 2, Lines 18 and depicts in Figure 4 that only one row is read out of the image sensor at a time and transferred to the storage register (33). Elabd et al teaches on Column 5, Lines 14-40 the use of a dump drain (35) depicted in Figure 6A that is formed by gates (53,55,35 and 51) This is viewed by the examiner as a readout gate since the charge from the

image array needs to pass through the dump drain to be stored in the storage register. Elabd et al further teaches on Column 2, Lines 60-68 and Column 5, Lines 28-35 that the rows of image data transferred to the storage register (33) can be combined using storage site (59) to permit rows to be combined for less detail and a variety of other options. Therefore, in the embodiment discussed on Column 2, Lines 60-68, multiple rows of data are combined in storage register (33) and the then combined pixel value is transferred to transfer registers (17A and 17B). Therefore, transfer register 17A receives charges stored in even-numbered columns from the two mixed rows of image data. And transfer register 17B receives charges stored in odd-numbered columns from the two mixed rows of image data. Therefore, in the thinned readout mode the transfer registers concurrently read out image data from two rows of pixels (the two rows of data are mixed). Elabd et al teaches the use of a three dimensional array and therefore, teaches the use of vertical shift registers to vertically shift the image data. However, Elabd et al does not teach that the image array can be directly connected to accumulation gate without any vertical shift registers between them.

Hirmada et al teaches on Column 1, Lines 32-60 and depicts in Figure 1 the use of a linear image sensor in which the accumulation gate 29A is directly connected to the sensor array (22) via a readout gate (ROG). This is capable because the sensor array in Hirmada et al is a linear array and requires no vertical shift register. Linear image sensors are advantageous to use in document scanning systems.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to directly connect the linear sensor of Hirmada et al to the accumulation

gate of Elabd et al in order to allow the imaging system of Elabd et al to be used in an image scanning system in which a linear sensor is required.

20: As for Claim 16, Elabd et al teaches in Table 1 on Column 8, Lines 10-45 that the read-out gate and the accumulation gate are comprised of a same material.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Hannett whose telephone number is 571-272-7309. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on 571-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2622

JMH
January 4, 2007

VIVEK SRIVASTAVA
SUPERVISORY PATENT EXAMINER
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